CMOS Digital decoding IC for Compact Disc

SAA7341

FEATURES

- Analog front end (data slicer, phase detector, VCO)
- Demodulator and EFM decoding
- Subcoding microprocessor handshaking protocol
- Integrated programmable motor speed control
- Single/four wire motor operation option
- Bidirectional data bus to external SRAM (8k x 8 bits)
- Error correction and concealment functions
- IEC/EBU digital output
- 192 x oversampling via 2-stage digital filter
- 2nd order noise shaping
- One-bit DAC with 1.4 V (RMS)
- Attenuation, mute and de-emphasis functions
- Power-on reset and standby functions

GENERAL DESCRIPTION

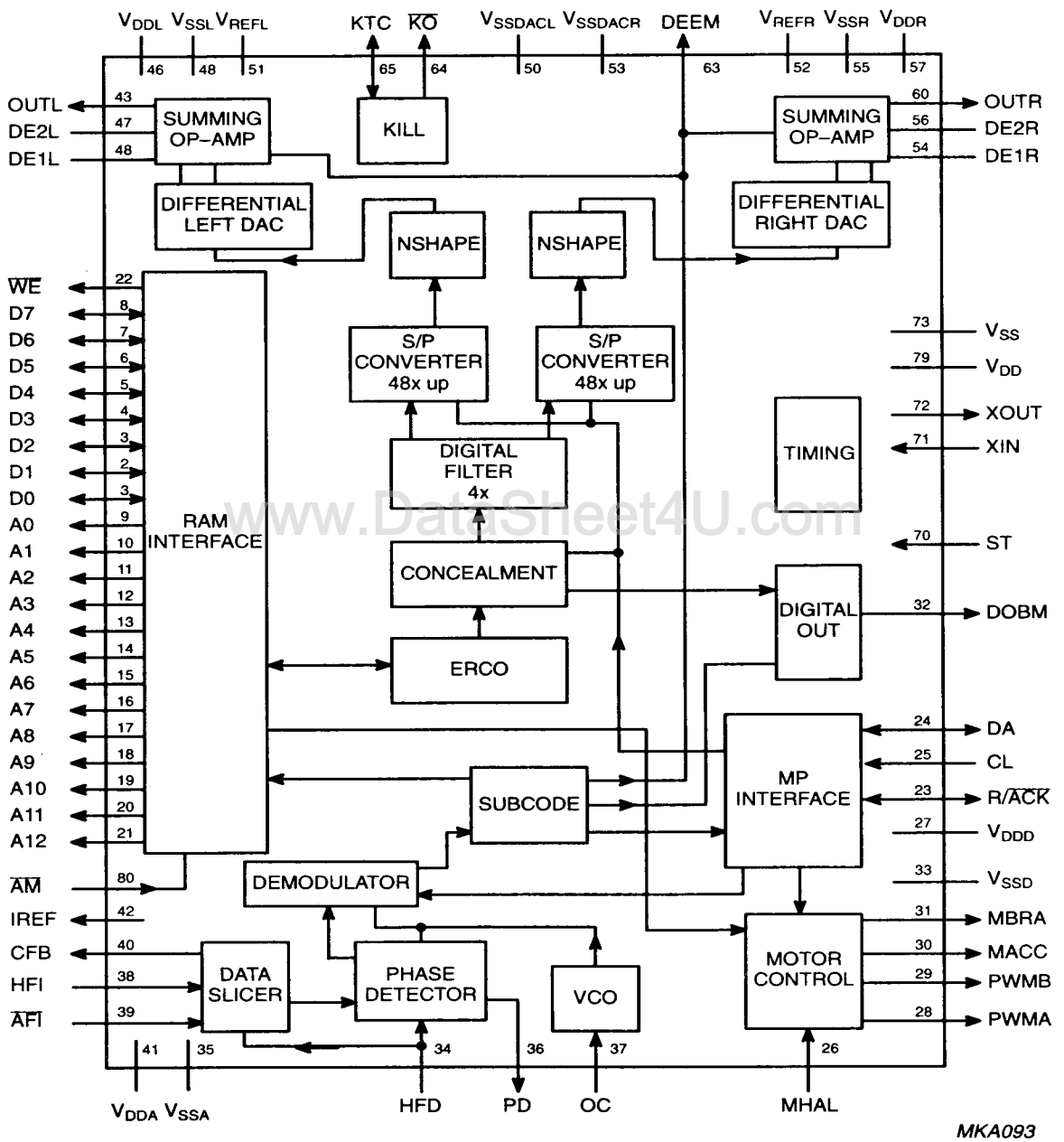
The SAA7341 incorporates the functions of decoding, digital filtering, and differential Digital-to-Analog conversion all on one CMOS IC. The device is specifically aimed at the mid-low end CD market, suitable for portable and car type applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.0	5.5	V
I_{DD}	supply current	-	60	-	mA
f_{XTAL}	crystal frequency range	15.24	16.9344	18.63	MHz
T_{amb}	operating ambient temperature range	−40	-	+85	°C
T_{stg}	storage temperature range	−55	-	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7341GP	80	QPF	plastic	SOT219



Test pins (numbers 66 to 69, 74 to 78) not shown

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D0 to D7	1 to 8	data inputs/outputs to external RAM
A0 to A12	9 to 21	address outputs to external RAM
$\overline{WE}$	22	write enable: output signal to external RAM (active LOW)
R/$\overline{ACK}$	23	request/acknowledge: input/output microprocessor interface; this pin has an open drain output with internal pull-up of 50 kΩ; input is debounced by two 4.2336 MHz clock cycles
DA	24	microprocessor interface data input/output line; input is debounced by two 4.2336 MHz clock cycles
CL	25	microprocessor interface clock input debounced by two 4.2336 MHz clock cycles
MHAL	26	Hall effect detector for motor: input for motor reversal, with internal pull-up of 50 kΩ
V_{DDD}	27	+5 V supply for digital audio output (DOBM) and motor speed control (MSC) output buffers
PWMA	28	pulse width modulated motor control acceleration signal: output active during acceleration; single ended mode output
PWMB	29	pulse width modulated motor control brake signal: output active during braking
MACC	30	motor accelerate signal output
MBRA	31	motor brake signal output
DOBM	32	biphase-mark digital audio output: this output conforms to the format defined by IEC 958
V_{SSD}	33	ground for digital audio output (DOBM) and motor speed control (MSC) outputs
HFD	34	high-frequency detector: when HIGH this input enables the fine frequency and phase detector outputs and also the feedback from the data slicer; this input has an internal pull-up of 50 kΩ
V_{SSA}	35	analog ground for front end
PD	36	phase detector: the phase detector output and fine/coarse frequency outputs are combined internally and the resultant signal controls the VCO frequency
OC	37	VCO control input
HFI	38	non-inverting data slicer input; normally AC-coupled to EFM data source
$\overline{HFI}$	39	inverting data slicer input; normally connected via external capacitor to ground of EFM data source
CFB	40	data slicer feedback output to capacitor: disabled when a data run length violation is detected or HFD is LOW to stop the slicing level from drifting
V_{DDA}	41	+5 V analog supply for front end
IREF	42	current reference output: reference current for internal curr ent sources, nominally 114 µA, requires external resistor connected to ground

SYMBOL	PIN	DESCRIPTION
OUTL	43	left channel output
n.c.	44	not connected
n.c.	45	not connected
V_{DDL}	46	+5 V analog supply for left channel integrator and operational amplifier
DE2L	47	pin 2 for external de-emphasis capacitor and resistor (left channel)
V_{SSL}	48	analog ground for left channel integrator and operational amplifier
DE1L	49	pin 1 for external de-emphasis capacitor and resistor (left channel)
V_{SSDACL}	50	analog ground for DAC (left channel)
V_{REFL}	51	internal reference voltage node for DAC left channel requiring an external decoupling capacitor
V_{REFR}	52	internal reference voltage node for DAC right channel requiring an external decoupling capacitor
V_{SSDACR}	53	analog ground for DAC (right channel)
DE1R	54	pin 1 for external de-emphasis capacitor and resistor (right channel)
V_{SSR}	55	analog ground for right channel integrator and operational amplifier
DE2R	56	pin 2 for external de-emphasis capacitor and resistor (right channel)
V_{DDR}	57	+5 V analog supply for the right channel integrator and operational amplifier
n.c.	58	not connected
n.c.	59	not connected
OUTR	60	right channel output
n.c.	61	not connected
n.c.	62	not connected
DEEM	63	output for external de-emphasis switches
$\overline{KO}$	64	output pulse (LOW) used to activate external kill circuit during power on/off
KTC	65	input/output connection to external capacitor used for the timing of the kill pulse at power on
TEST1 to 4	66 to 69	these output pins should be left open-circuit
$\overline{ST}$	70	standby mode, input active LOW. Internal 50 kΩ pull-up resistor
XIN	71	input from crystal oscillator or external clock input (16.9344 MHz typ.)
XOUT	72	output to clock crystal
V_{SS}	73	ground for digital section
TEST5	74	this output pin should be left open-circuit
TEST6 to 9	75 to 78	these input pins should be tied HIGH
V_{DD}	79	+5 V supply for digital section
$\overline{AM}$	80	this input pin is normally held HIGH; should track loss occur this pin should be taken LOW and then the data is corrupted before the FIFO stage; this pin has an internal 50 kΩ pull-up resistor

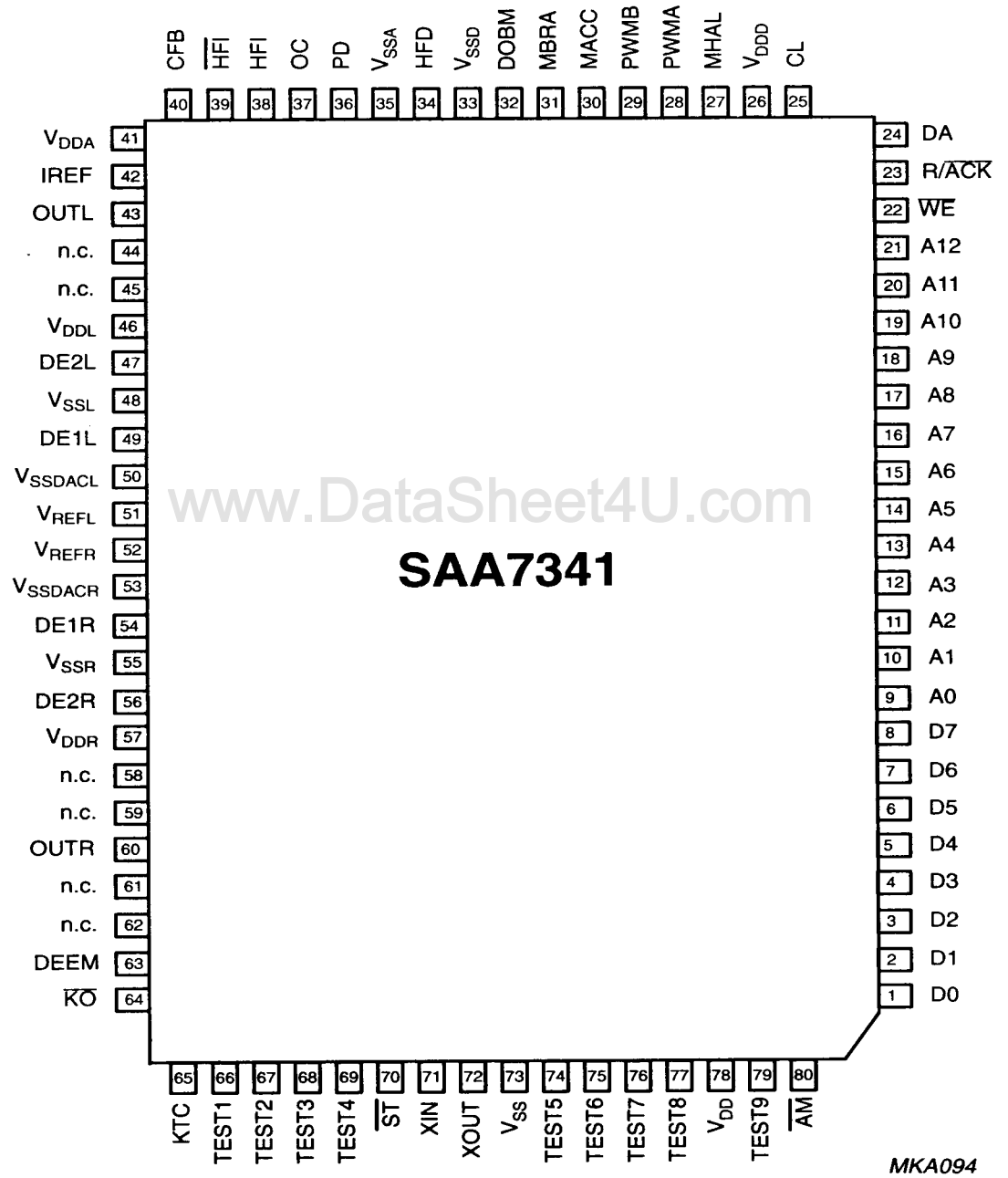


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Analog Front-End

The analog front-end contains the following functions: a data slicer, a VCO clock generator, fine and coarse frequency current switches and a current reference circuit.

The HFI input signal is converted to a digital signal by the data slicer. This is an adaptive level detector which relies on the DC-free nature of the modulation system to determine the optimum slicing level. When a signal drop-out is detected either externally via the HFD input or internally via the data run length violation detector, the feedback around the data slicer is disabled to stop the slicing level drifting.

Two (digital) frequency detectors and the phase detector provide coarse and fine control signals for the internal phase-locked-loop (PLL). The voltage controlled oscillator (VCO) is totally integrated, the frequency being dependent on the voltage at the OC pin. A coarse frequency detector compares the VCO frequency with the crystal clock and if necessary pulls the VCO to within the capture range of the fine frequency detector. This second detector uses data run length violations to pull the VCO further to within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled.

A separate current reference circuit is built in. An external resistor is needed at pin IREF (connected to V_{SS}).

Demodulator

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected master counter is only reset if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the master counter. During track jumping it is necessary to allow the master counter to free run to minimise interference to the motor speed controller. An out-of-lock signal indicates that no sync coincidences are found within a certain period. This signal enables the fine frequency detector when the HFD input is HIGH. When HFD is LOW the working of the fine frequency detector is disabled.

The EFM (eight-to-fourteen modulation) decoder converts each symbol into one of 256 8-bit binary words which are passed across the clock interface to the subcode section. An additional output from the EFM decoder senses both extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe is also passed across the clock interface.

Subcoding

The subcode section runs on a clock divided from the crystal clock while the demodulator uses the VCO clock.

The demodulator output word and timing signals are latched on an enable signal derived from the demodulator data sync. The output of this latch either goes to the subcode processor (first byte of frame) or goes to the external RAM during a WRITE1 cycle. Due to the extended accessibility of the external RAM for the WRITE1 cycles compared to previous decoders a pre-FIFO is not needed. There are 72 time slots to write an EFM data frame of 32 bytes. The nominal period between two bytes delivered by the EFM decoder is 3.93 µs. the longest period between two WRITE1 slots is 2.13 µs.

The Q-channel processor of the subcoding section accumulates a subcoding word of 96 bits from the Q-bit of the subcoding symbol. It performs a cyclic redundancy check (CRC) using up 16 bits. If the CRC is good and the data is requested by the external processor the remaining 80 bits are put on the DA output on an external clock (CL).

The de-emphasis control signal is derived from 1 bit of the CRC checked Q-channel. This goes to DEEM output. A de-bounce is added for extra protection.

Subcode words (without the P-bit) are clocked to the digital output section together with a sync flag and a CRC result flag. They are fed into the user channel of the DOBM output signal. The control bits of a Q-frame are also copied to the first four bits of a channel status block. Conforms to Annex A of IEC 958.

Microprocessor Interface

The SAA7341 interfaces with a microprocessor by means of a 3-line bus consisting of a request/acknowledge line (R/$\overline{\text{ACK}}$), a clock line (CL) and a data line (DA). The microprocessor can request Q-data from the SAA7341 or send control data for the motor speed control section.

Q-FRAME OUTPUT PROTOCOL

As long as the R/$\overline{\text{ACK}}$ line is held LOW by the microprocessor it can write control information to the SAA7341.

A Q-frame request is carried out when CL is HIGH by releasing the R/$\overline{\text{ACK}}$ line which should then go HIGH due to the pull-up resistor internal to the SAA7341. Figs 5 and 6 show the timing waveforms.

The SAA7341 is continually collecting Q-channel data and if it detects that R/$\overline{ACK}$ is HIGH it will hold the first frame of Q-data for which the CRC is good. It will then pull down R/$\overline{ACK}$ (acknowledge) and switch on the DA output. The microprocessor provides the clock to the CL input. After the first HIGH-to-LOW transition of CL, the SAA7341 will allow the R/$\overline{ACK}$ line to go HIGH. At the following HIGH-to-LOW transitions of CL the next Q-channel data bits will become available at the DA pin. As soon as the microprocessor has enough data (not necessarily 80 bits) it will pull R/$\overline{ACK}$ down again and the SAA7341 will disable DA and start collecting new Q-channel data.

If the microprocessor does not give a clock signal within 10.88 ms from the start of the acknowledge (R/$\overline{ACK}$ LOW) then the SAA7341 will reset the acknowledge signal and allow the R/$\overline{ACK}$ line to go HIGH again. After that the microprocessor still has 2.3 ms to accept the data. After a further 13.3 ms (typ.) the SAA7341 will have received a new Q-channel frame and if the CRC check is good a new acknowledge will be given.

Microprocessor data write protocol

The microprocessor can write data words into the 4-bit control registers of the SAA7341 when R/$\overline{ACK}$ is LOW. An 8-bit data burst on DA clocked with the positive edge of CL contains a 4-bit address (MSB first) and 4 bits of control data. It can be followed immediately by another burst of data without taking R/$\overline{ACK}$ HIGH.

Internally the receiver is reset when R/$\overline{ACK}$ is HIGH. The receiver will also be reset at stand-by and power-on. During the initialisation procedure the R/$\overline{ACK}$ line is held LOW by the SAA7341. When R/$\overline{ACK}$ becomes HIGH the SAA7341 is ready to receive data from the microprocessor.

A 2 bit debounce mechanism on CL and on the DA input protects the receiver against spikes.

Internal Control Registers

A set of 8 control registers hold the different system parameters for all types of applications. One register is used to control the audio processing (e.g. mute, −12 dB attenuation). Other registers hold the parameters for the spindle motor control loop.

Table 1 Internal control registers; the initial values are loaded during power-on

ADDRESS				DATA				INITIAL STATE			
msb			lsb								
A3	A2	A1	A0	D3	D2	D1	D0				
0	0	0	0	DIM	ANM	ATT	CRIB	1	1	1	1
0	0	0	1	TIM3	TIM2	TIM1	TIM0	0	1	1	1
0	0	1	0	OFS3	OFS2	OFS1	OFS0	0	0	0	0
0	0	1	1	OFS7	OFS6	OFS5	OFS4	1	1	1	0
0	1	0	0	STOP	STRT	STPM	PWMM	1	1	1	1
0	1	0	1	LEV3	LEV2	LEV1	LEV0	0	0	1	1
0	1	1	0	VEL	POS	INT	INH	1	1	1	1
0	1	1	1	GAIN3	GAIN2	GAIN1	GAIN0	0	0	0	0

Where:

DIM Digital mute. When HIGH the DAC outputs and the sample data in the digital output (DOBM) will be muted.

ANM Analog mute. When HIGH only the DAC output is suppressed. The digital output (DOBM) is not affected.

ATT Attenuate (-12dB). When HIGH the DAC outputs and sample data in the digital output (DOBM) are attenuated.

CRIB Counter reset inhibit. When CRIB is LOW the Demodulator master counter will free run.

The following signals are used in the motor control section:

TIM [3:0] Start time selector. The selected start time is loaded in a timer which determines the duration of the start pulse.

OFS [3:0] Low order nibble of accumulator offset.

OFS [7:4] High order nibble of accumulator offset.

STOP STOP signal.

STRT START signal.

STPM STOP Mode selection.

PWMM PWM mode selection.

LEV [3:0] Start/stop level selection. The selected level is the modulus of a constant value injected into the motor control output processor during start or stop. The sign is controlled by STRT/STOP (negative for STRT).

VEL Velocity branch selection. When HIGH the output of the velocity branch is added with the output of other selected branches.

POS Position branch selection. When HIGH the output of the position branch is added with the output of other selected branches.

INT Position integrator branch selection. When HIGH the output of the integrator is added with the output of other selected branches.

IHB Integrator hold. Signal to switch off the input of the integrator. When IHB is LOW the position information is added to the contents of the accumulator once per frame.

GAIN [3:0] Loop gain selection. The loop gain can be selected according to the application.

Error Correction (ERCO)

The error corrector (ERCO) carries out t = 1, e = 0 error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. The strategy t = 1, e = 0 means that the ERCO can correct one erroneous symbol per frame and detect all erroneous frames. As e = 0, no erasure corrections (to flagged symbols) are carried out.

The error corrector also contains the Flag Processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags. There are no input flags for C1.

Concealment

The concealment section performs the following functions:

- Up to 6 sample interpolation in each channel to conceal erroneous data flagged by the error corrector. When more than 6 samples are corrupted the last good value will be held.
- Attenuation of −12 dB.
- Digital mute.
- Signal conditioning for filter section.

RAM Interface

The RAM interface section generates addresses for the external RAM in order to carry out the processing necessary to supply data in the correct manner to ERCO (for both C1 and C2 correction processes) and subsequently to the concealment section.

The data path involves entering and leaving the external RAM 3 times. These operations are:

- FIFO and "small d" de-interleaving between SUBCODE and C1.
- "Large D" de-interleaving between C1 and C2.
- De-scrambling between C2 and CONCEALMENT.

In addition to the data operations, flags generated by the C1 and C2 correction processes are also processed by the RAM interface section. C1 output symbol flags receive the same de-interleaving processing as C1 output data, before being supplied to C2. C2 flags are also passed through the de-scrambling process but receive one frame less delay than the corresponding C2 output data before being supplied to the concealment section. This enables the concealment section to initiate a jump action by the RAM interface to fetch the next good sample from the RAM when the flagged data needs to be interpolated.

External RAM Timing

The external RAM is an 8k x 8 static CMOS RAM. An SAA7341 RAM address cycle takes nominally 236.2 ns. The write cycles are $\overline{WE}$ controlled. The RAM interface timing waveforms are shown in Fig.4.

Digital Audio Output (DOBM)

The biphase-mark digital output signal is according to the format defined by IEC 958. The clock frequency for this section is 5.6448 MHz (one third the crystal frequency).

Format

The digital audio output consists of 32 bit words ("subframes") transmitted in biphase-mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384.

Each word contains information as shown in Table 2.

Table 2 Word information

PARAMETER	BIT	DESCRIPTION
sync	1 to 4	-
auxiliary	1 to 4	not used; always zero
audio sample	9 to 28	first 4 bits not used (always zero); two's compliment; LSB = bit 13, MSB = bit 28
validity flag	29	valid = logic 0
user data	30	used for subcode data (Q-W)
channel status	31	control bits and category code
parity bit	32	even parity for bits 5 to 31

SYNC

The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns indicate the following situations:

Sync B	Start of a block (384 words), word contains left sample.
M	Word contains left sample (no block start).
W	Word contains right sample.

AUDIO SAMPLE

Left and right samples are transmitted alternately. Audio samples are available for DOBM in the concealment section after interpolation, attenuation and muting.

VALIDITY FLAG

Audio samples are flagged when they are not the original samples after error correction. The validity flag is logic 1 when the audio sample is the result of interpolation, muting or attenuation.

USER DATA

Subcode bits Q until W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.

CHANNEL STATUS

The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is as shown in Table 3.

Table 3 Bit assignment

PARAMETER	BIT	DESCRIPTION
control	1 to 4	copy of CRC checked Q-channel
reserved mode	5 to 8	always zero
category code	9 to 16	CD: bit 9 = logic 1, all other bits = logic 0
remaining	17 to 192	always zero

DIGITAL FILTER

The digital filter is a 4 times oversampling recursive interpolation filter. It is constructed of 2 cascaded bireciprocal wave low-pass filters operating on a clock frequency of 4.2336 MHz. The sampling rates are 44.1 kHz and 88.2 kHz respectively.

The filter receives 16 bit samples from the concealment section. The output of the filter is scaled in such a way that a sinewave with maximum amplitude at the input can never cause overflow in the noise shaper.

The serial outputs of the digital filter contain 20 bit data samples at a rate of 176.4 kHz. Left and right samples are converted to parallel and held for 48 cycles of 8.4672 MHz.

The analog mute signal set via a microprocessor control register is synchronized to a sample. When it is HIGH the input of the converter is zero.

The second order digital noise shaper operates at a rate of 8.4672 MHz which is 192 times the sampling frequency. Overflow is prevented by a clipping mechanism. The 1-bit output of the noise shaper is connected to the DAC. There are two noise shapers, one for each channel.

Table 4 Filter characteristics

PARAMETER	VALUE (dB)	FREQUENCY (kHz)
passband ripple	−0.1 to 0	0 to 20
transition band	monotonic −3 −14	20 to 26 22.05 24
stopband attenuation	<−30 <−35	26 to 88.2 40 to 65
roll off due to sinx/x	0.18	-

D/A Conversion

The 1-bit output of the noise shaper is converted to an analog signal by a 1-bit differential switched-capacitor integrator.

The differential outputs are summed by an internal operational amplifier.

Kill, Power-on Reset and Standby Functions

A kill signal is available from the $\overline{KO}$ output to activate an external kill circuit when required.

A power-on reset signal is derived from the external capacitor on KTC to initialize some of the internal control signals.

The SAA7341 can be put in standby mode to achieve silence at the outputs (except for XOUT) when the CD function in a combination player (music centre) is switched off. Also interference and power consumption will be minimized in the standby mode.

Spindle Motor Control Section

The motor control section uses the FIFO phase information from the RAM addressing section and disc speed information to calculate the motor control output signals. This calculation is performed at a rate of 7.35 kHz. The master clock of this section is 4.2336 MHz.

The motor control loop contains three branches : velocity, position and integrated position. These branches can be switched off independently by the microprocessor.

The outputs that drive the motor are MACC, MBRA, PWMA and PWMB. MACC and MBRA are active (HIGH) when the motor has to be accelerated or braked respectively. PWMA and PWMB are pulse width modulated signals with a frequency of 22.05 kHz of which the duty cycle controls the strength of the acceleration (PWMA) or braking effect (PWMB). In a second selectable PWM-mode only one output (PWMA) is used.

By means of a 4-bit control register the following 5 modes of operation are possible :

- PASSIVE (motor control loop switched off)
- START (accelerate for a set time before PLAY takes over)
- PLAY (PLL motor on)
- BRAKE (braking unit told otherwise by microprocessor)
- STOP1 (braking until disc stopped then PASSIVE)

A block diagram of the motor control loop, including the microprocessor registers, is shown in Fig.8.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage; note 1	−0.5	+6.5	V
V_I	maximum input voltage	−0.5	V_{DD} + 0.5	V
I_{REFabs}	input current, IREF only	-	+2	mA
I_{IK}	DE input diode current	-	±20	mA
V_O	output voltage	−0.5	+6.5	V
I_O	output current		±10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−40	+85	°C
V_{es}	electrostatic handling; note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0; T_{amb} = 25° C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	-	60	-	mA
V_{SS}, V_{SSD}, V_{SSA}, V_{SSL}, V_{SSR}	ground	note 1	0	-	0	V
V_{DD}, V_{DDD}, V_{DDA}, V_{DDL}, V_{DDR}, V_{DDR}	positive supply voltage	note 1	4.5	5	5.5	V
Digital inputs						
$\overline{AM}$, $\overline{ST}$, MHAL, HFD						
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3	V
V_{PU}	pull-up voltage	I_I = 0 µA	2.0	-	V_{DD} + 0.3	V
C_I	input capacitance		-	-	10	pF
R_I	internal pull-up resistor		15	50	100	kΩ
CL						
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	-	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance		-	-	10	pF
XIN (EXTERNAL CLOCK)						
V_{IL}	input voltage LOW		−0.3	-	1.5	V
V_{IH}	input voltage HIGH		3.5	-	V_{DD} + 0.3	V
I_{LI}	input leakage current		−10	-	+10	µA
C_I	input capacitance		-	-	10	pF
Digital Input/Output						
D0 TO D7						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3V	
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	-	+10	µA
C_I	input capacitance		-	-	10	pF
DA						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	100	pF
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3V	
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	-	+10	µA
C_I	input capacitance		-	-	10	pF
R/$\overline{ACK}$						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
C_L	load capacitance		-	-	100	pF
R_I	internal pull-up resistor		15	50	100	kΩ
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3	V
V_{PU}	pull-up voltage	I_I = 0 µA	2.0	-	V_{DD} + 0.3	V
C_I	input capacitance		-	-	10	pF
Digital Outputs						
A0 TO A12						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
I_{LO}	3-state leakage current	V_O = 0 to V_{DD}	−10	0	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{WE}$, DEEM						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
DOBM (SEE FIG. 3 FOR LOAD)						
$V_{O(p-p)}$	voltage across a 75 Ω load (peak-to-peak value)		0.4	-	0.6	V
MACC, MBRA						
V_{OL}	output voltage LOW	I_{OL} = +50 µA	0	-	0.3	V
I_{OH}	output current HIGH (constant source current)	V_O = 0 to 2 V	-	–1.5	-	mA
PWMA, PWMB						
V_{OH}	output voltage HIGH	I_{OH} = –50 µA	V_{DD} - 0.3	-	V_{DD}	V
I_{OL}	output current LOW (constant sink current)	V_O = 3 to V_{DD}	-	1.5	-	mA
Crystal Oscillator						
XIN, XOUT						
f_{XTAL}	crystal frequency		15.24	16.9344	18.63	MHz
g_m	mutual conductance at 100 kHz		1.5	-	-	mS
A_V	small signal voltage gain	$A_V = g_m.R_O$	3.5	-	-	V/V
C_I	input capacitance		-	-	10	pF
C_{FB}	feedback capacitance		-	-	5	pF
C_O	output capacitance		-	-	10	pF
Reference Voltage outputs						
VREFL, VREFR						
V_R	voltage reference		-	2.5	-	V
OUTPUT PERFORMANCE						
$V_{AO(RMS)}$	output level (RMS value)	note 2	-	1.4	-	V
S/N	signal-to-noise ratio	0 dB input	90	-	-	dB
THD	total harmonic distortion	0 dB/1 kHz	-	-	–70	dB
	(plus noise)	–10 dB/1 kHz	-	–80	-	dB
	channel matching	0 dB/1 kHz	–0.25	0	+0.25	dB
	crosstalk		-	–90	-	dB
PSRR	power supply rejection ratio		-	40	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Kill Circuit						
INPUT/OUTPUT: KTC						
	KTC switching level	KTC rising	-	3.0	-	V
		KTC falling	-	2.0	-	V
V_{OL}	output voltage LOW	I_{OL} = 0	0	-	0.4	V
R_I	internal discharge resistor	KTC = LOW	-	2	-	kΩ
I_{OH}	output current HIGH		-	10	-	µA
OUTPUT: $\overline{KO}$						
R_I	internal pull-down resistor		-	50	-	kΩ
V_{OH}	output voltage HIGH	I_{OH} = 0	V_{DD} - 0.2	-	-	V
V_{TK}	supply threshold for power on		-	1	-	V
V_{TPD}	supply threshold for power down		-	4.6	-	V
V_{HPD}	hysteresis of V_{TPD}		0	-	200	mV
Timing (note 3)						
RAM INTERFACE (SEE FIG. 4)						
t_{acc}	read access time (for external RAM)		-	-	150	ns
t_{wp}	write enable pulse		100	-	-	ns
t_{as}	address set-up time		0	-	-	ns
t_{wtz}	delay from falling edge of $\overline{WE}$ to data bus going low impedance	XIN = 16.9 MHz XIN = 18.6 MHz	35 30	- -	- -	ns ns
t_{wr}	write recovery time from rising edge of $\overline{WE}$		20	-	-	ns
t_{dw}	data valid before end of write		50	-	-	ns
t_{dh}	data hold time from rising edge of $\overline{WE}$		5	-	-	ns
MICROPROCESSOR INTERFACE (SEE FIGS 5, 6 AND 7)						
t_{an}	access time normal mode	note 4	0	-	n x 13.3	ms
t_{ar}	access time refresh mode	note 4	13.3	-	n x 13.3	ms
t_{da}	CL to RA acknowlege delay		-	0.9	2.0	µs
t_{rh}	CL to RA request hold time		2.0	-	-	µs
t_{cl}	CL input LOW time		2.0	-	-	µs
t_{ch}	CL input HIGH time		2.0	-	-	µs
t_{dd}	CL to DA delay time		-	0.9	2.0	µs
t_{ak}	acknowledge time	note 5	-	-	10.88	ms
t_{ah}	data hold time after acknowledge	note 6	2.31	-	-	ms
t_{ds}	microprocessor data set-up time to positive edge of CL		1.0	-	-	µs

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0; T_{amb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{dh}	microprocessor data hold time after positive edge of CL		2.0	-	-	µs
t_{drw}	delay to write after read		2.0	-	-	µs
t_{dwr}	delay to read after write		2.0	-	-	µs

Notes to the characteristics

1. All $V_{SS's}$ and all $V_{DD's}$ must be connected back to the ground and positive terminals of a single supply, respectively.
2. Maximum load recommended on OUTL, OUTR, is 5 kΩ, 100 pF. Device measured with external components shown in recommended application diagram (Fig.9). Maximum digital code.
3. Timing reference voltage levels are 0.8 V and 2.0 V.
4. Q-channel access times are dependent on the parity check on the Q channel data frame; n = the number of cycles until data is valid.
5. The acknowledge time is the time for which the SAA7341 will hold R/$\overline{ACK}$ LOW without the microprocessor driving CL LOW. The time is related to the frequency of the incoming data, and is therefore dependent on the frequency of the demodulation section. The value given is for demodulator operating at a nominal frequency of 4.32 MHz.
6. This is the amount of time for which the microprocessor can still successfully access the Q channel data after the SAA7341 has released R/$\overline{ACK}$ without CL going LOW. Again the time given is for demodulator operating at a nominal frequency of 4.32 MHz.

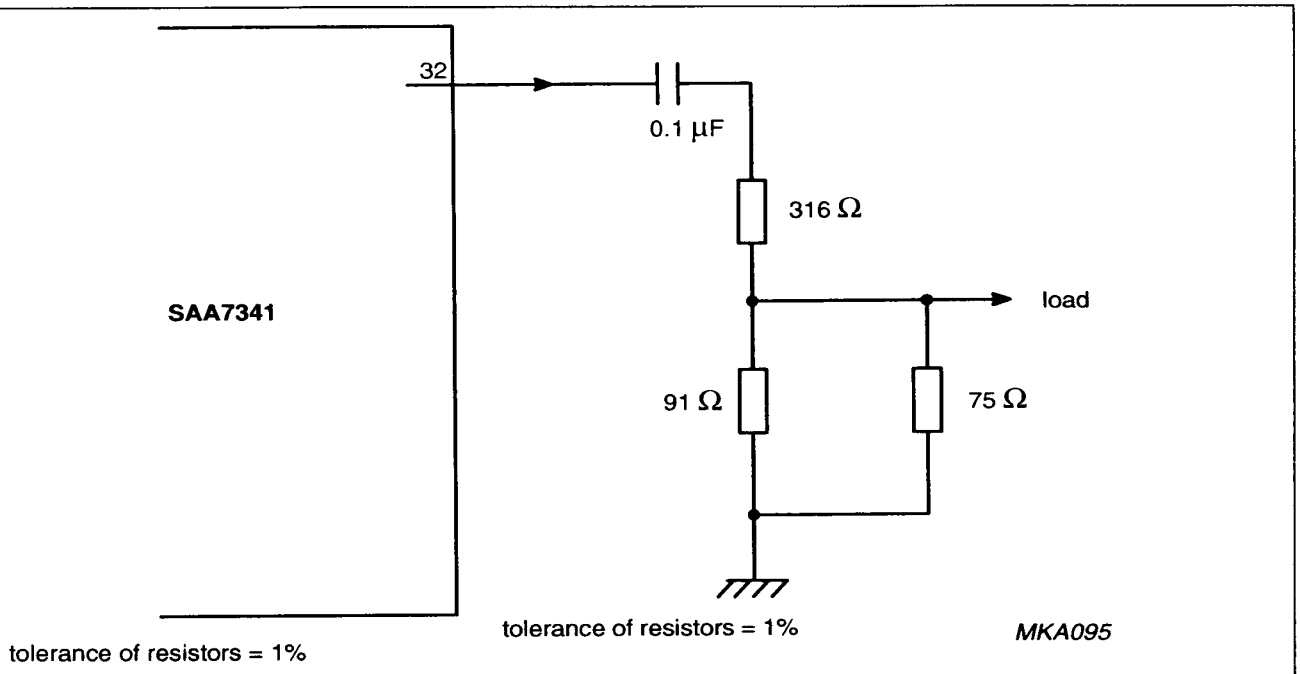


Fig.3 Digital audio output load.

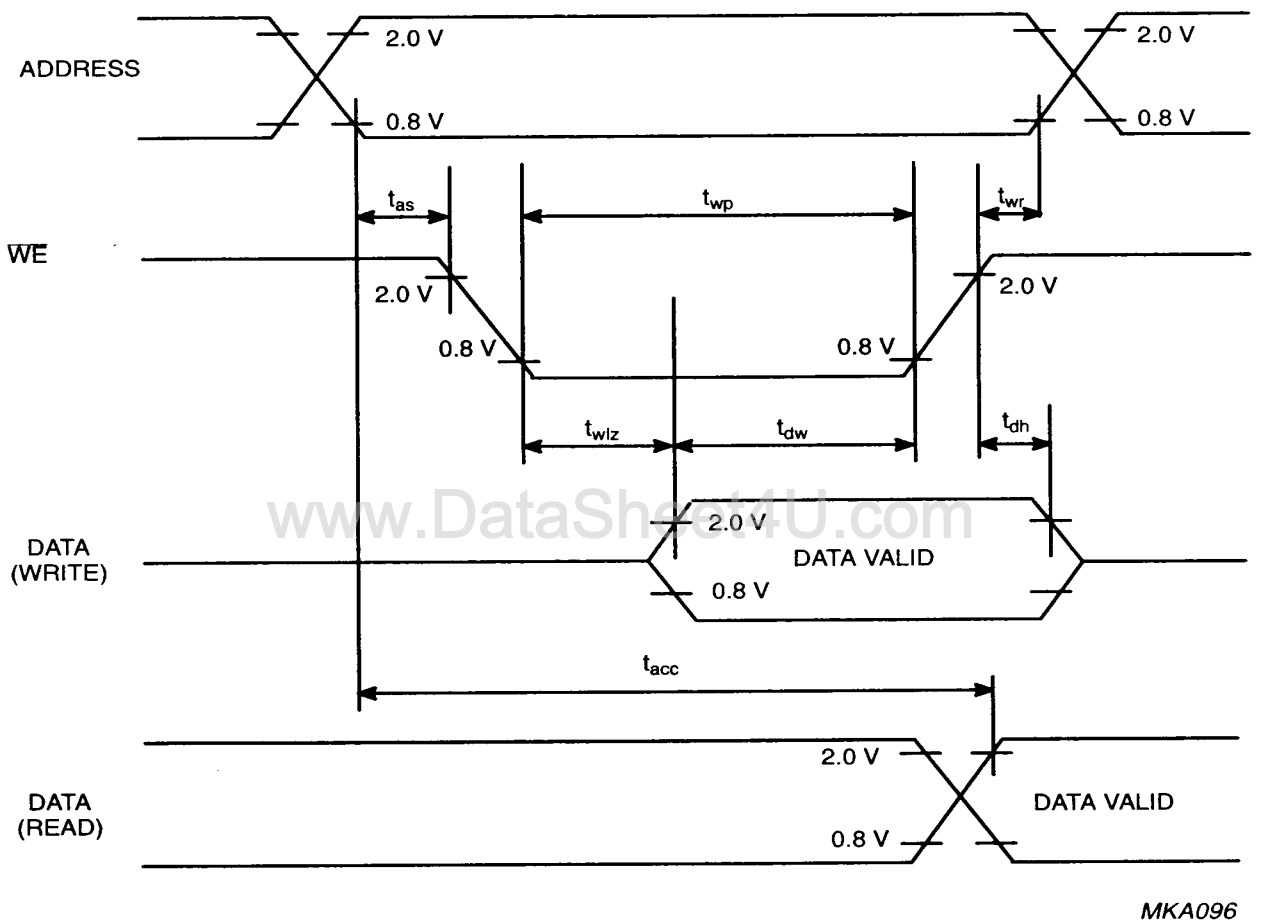


Fig.4 RAM interface timings.

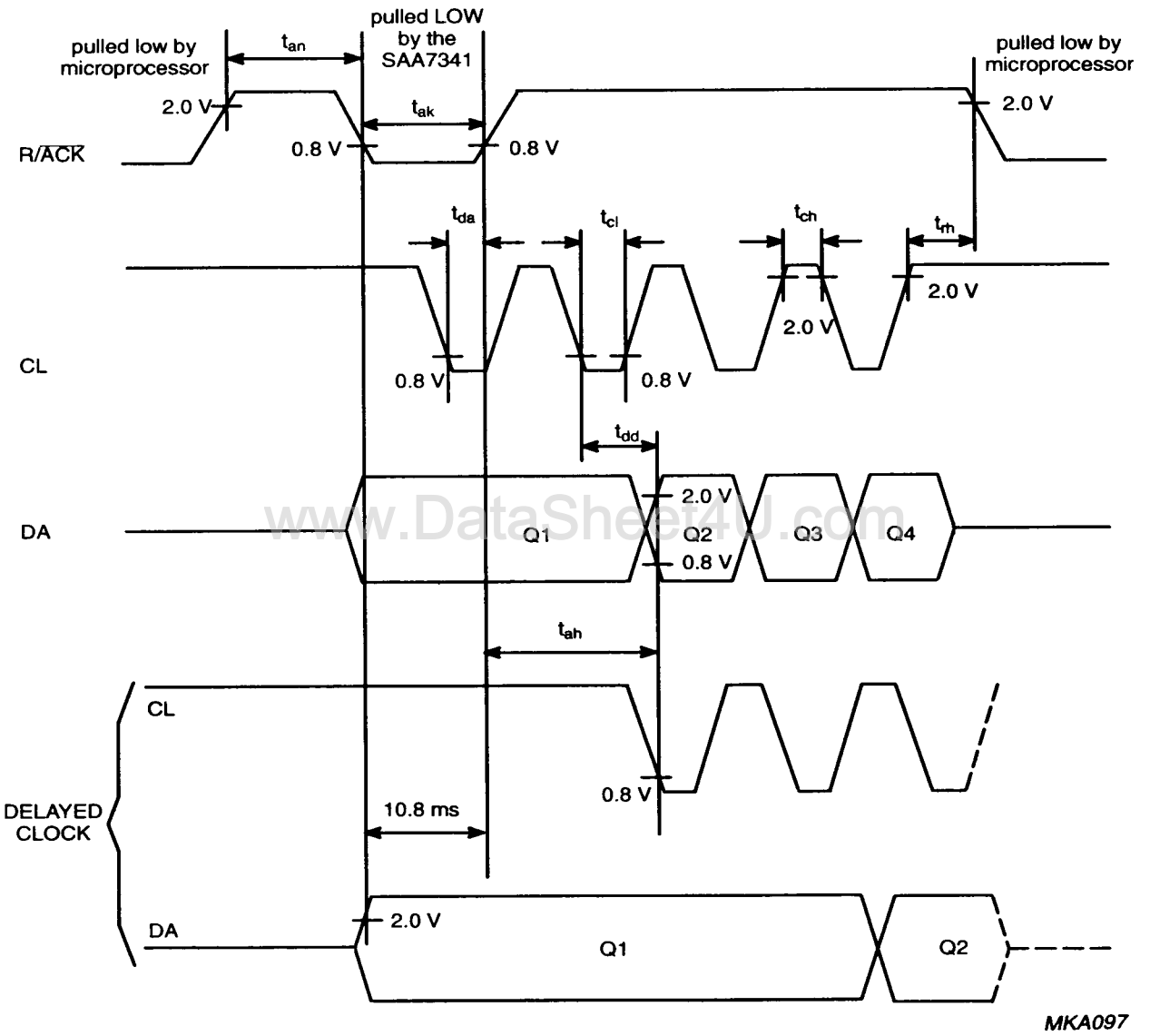


Fig.5 Q-channel timing wave forms (read mode).

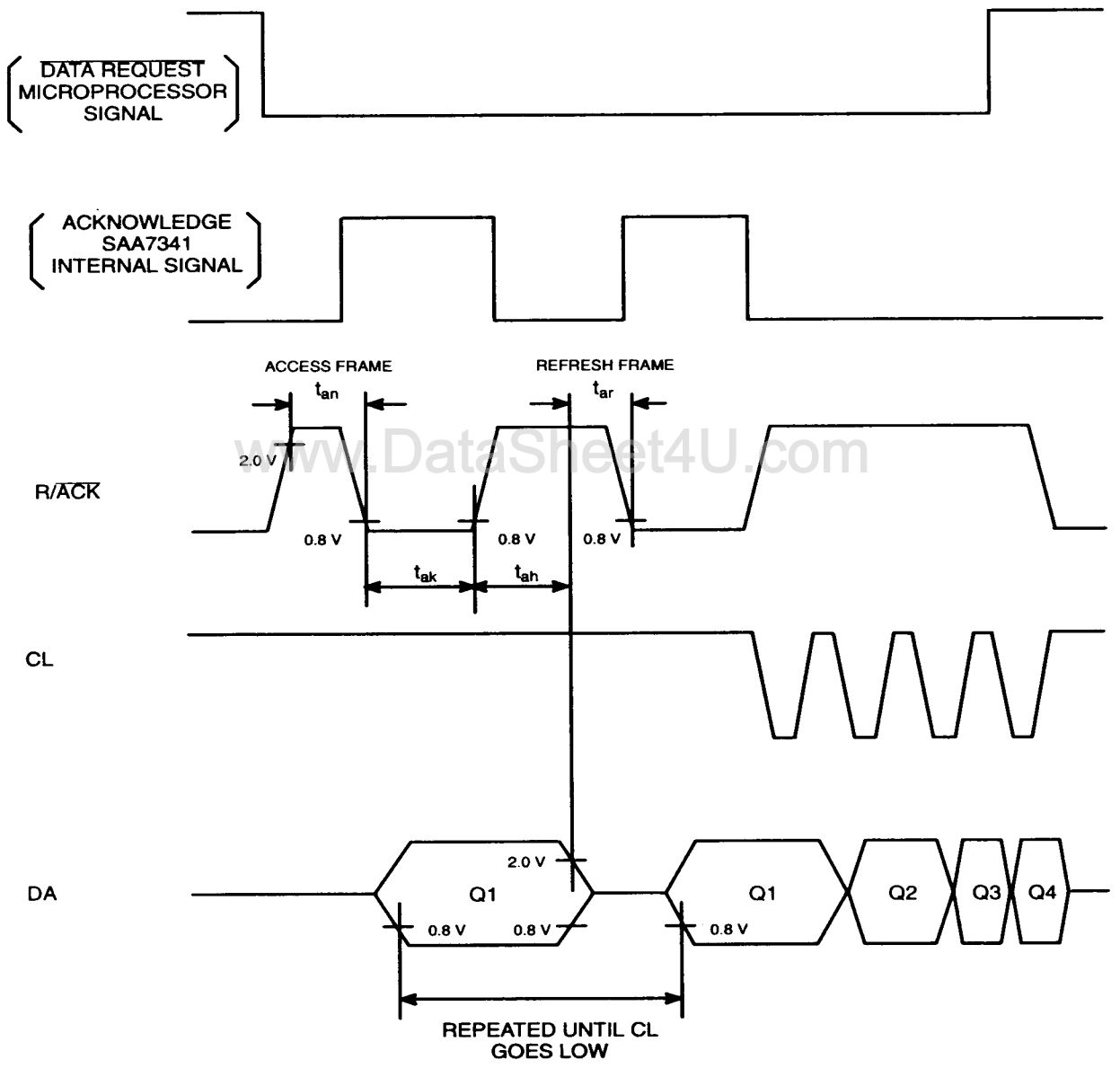


Fig.6 Q-channel timing waveforms (refresh mode).

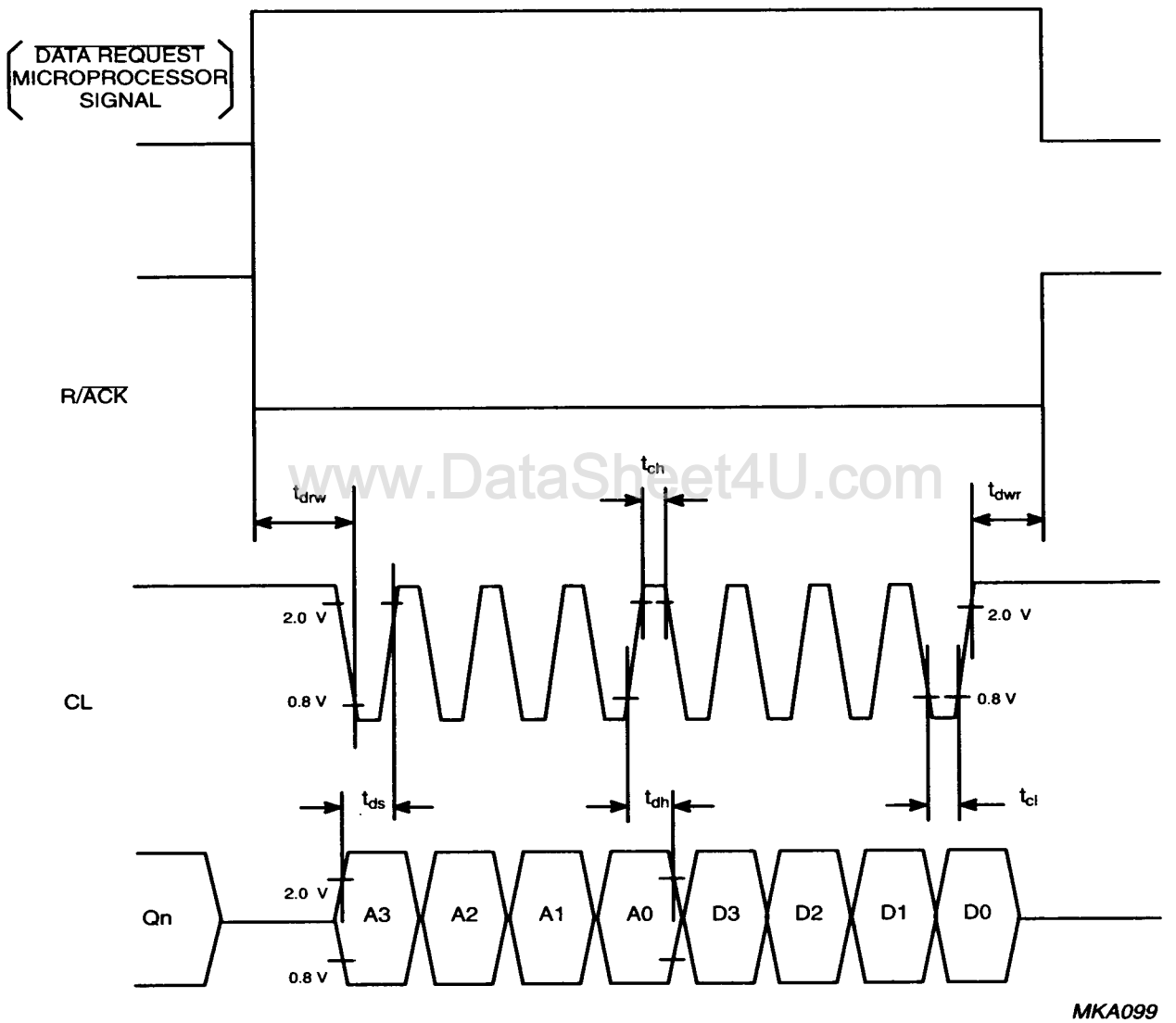


Fig.7 Microprocessor interface write mode.

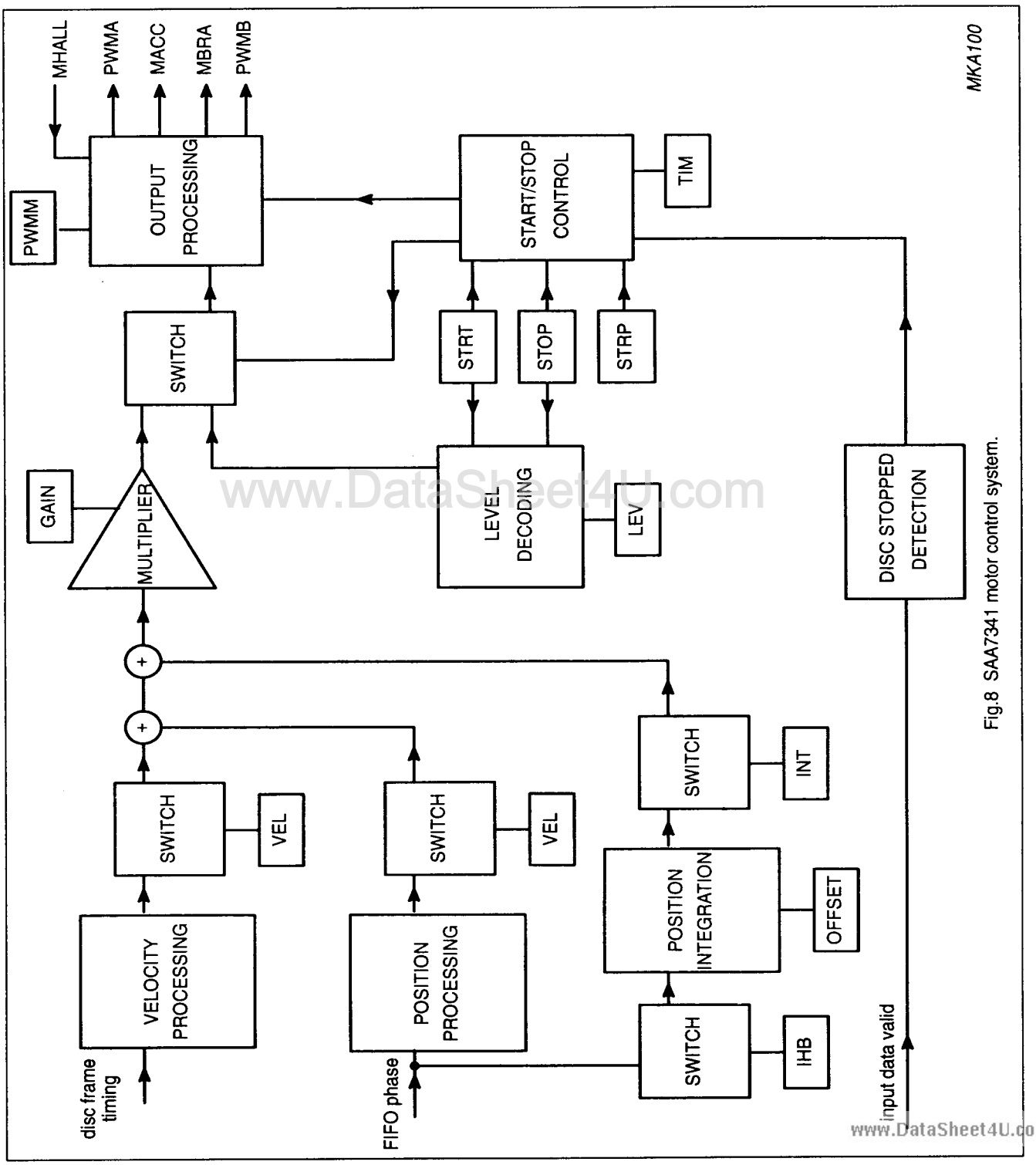


Fig.8 SAA7341 motor control system.

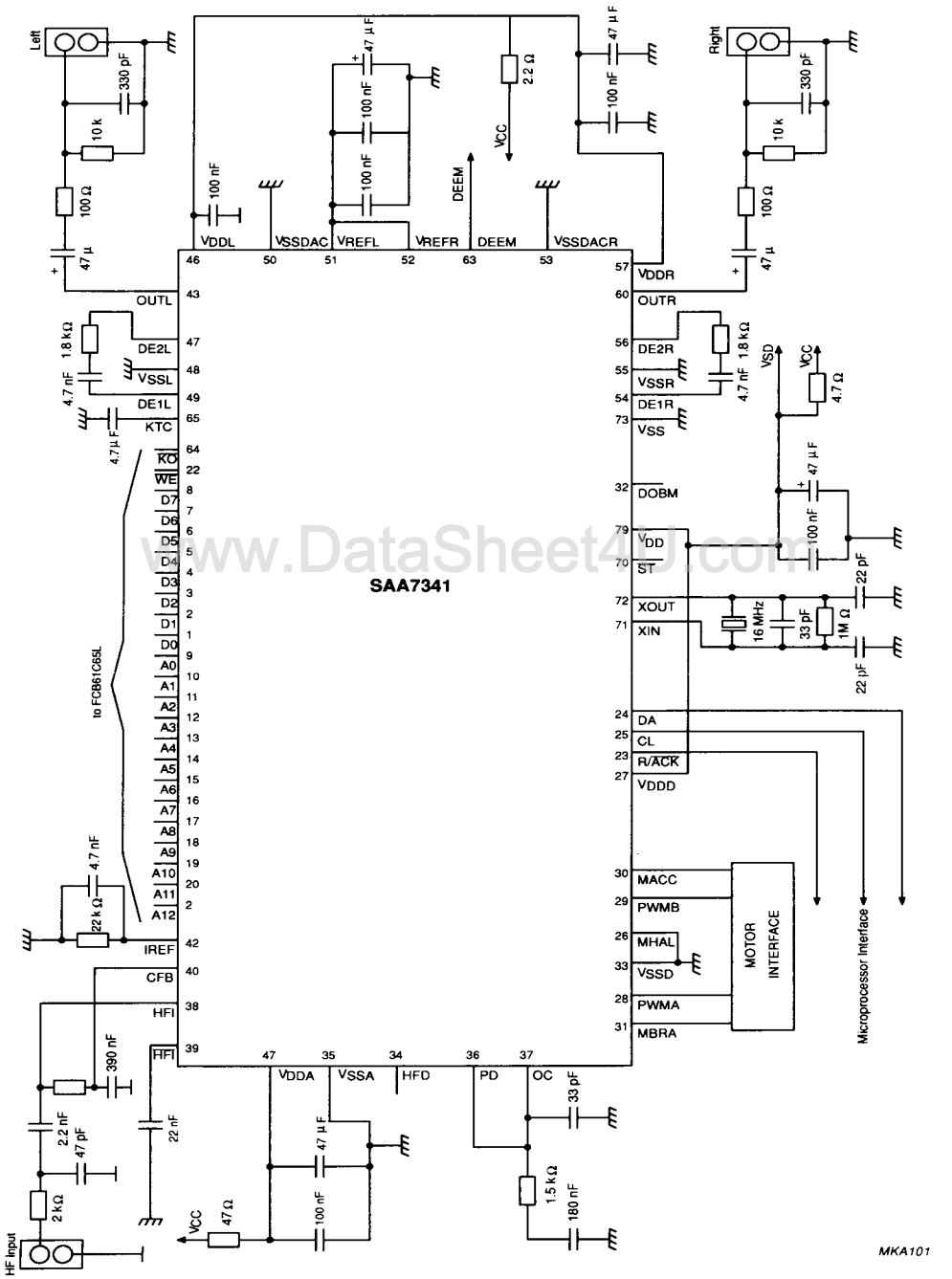


Fig.9 SAA7341 application circuit.

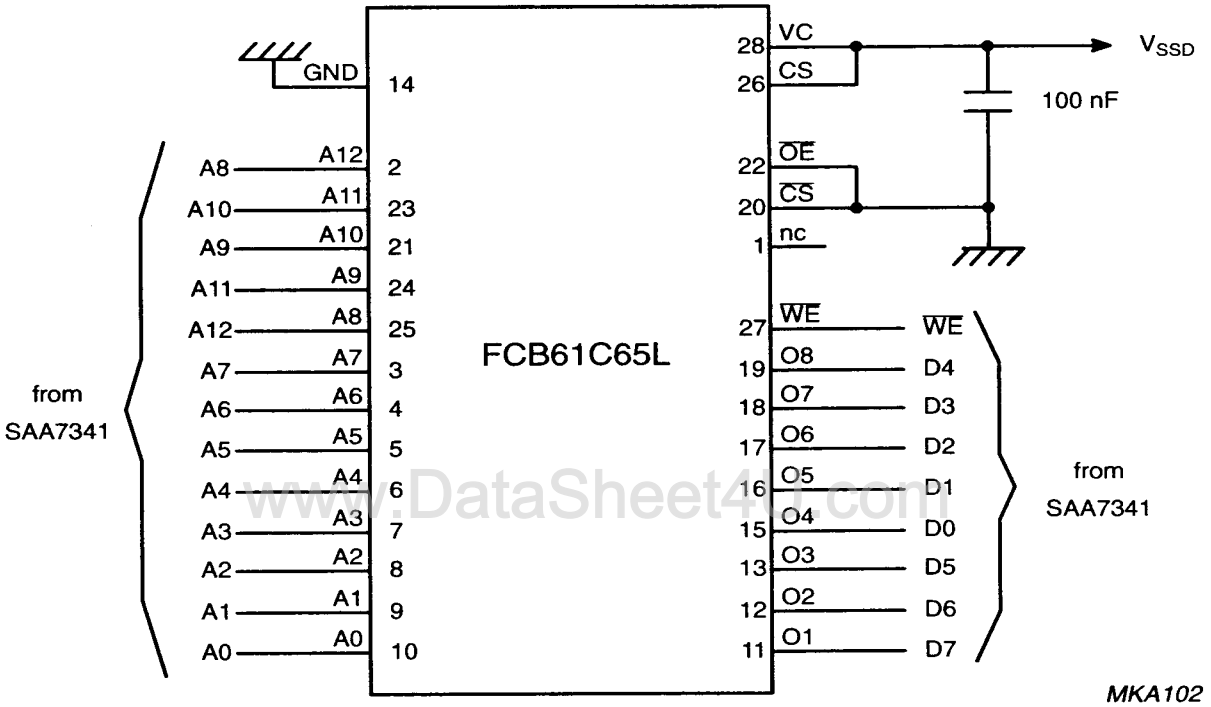


Fig.10 SRAM FCB61C65L configuration.

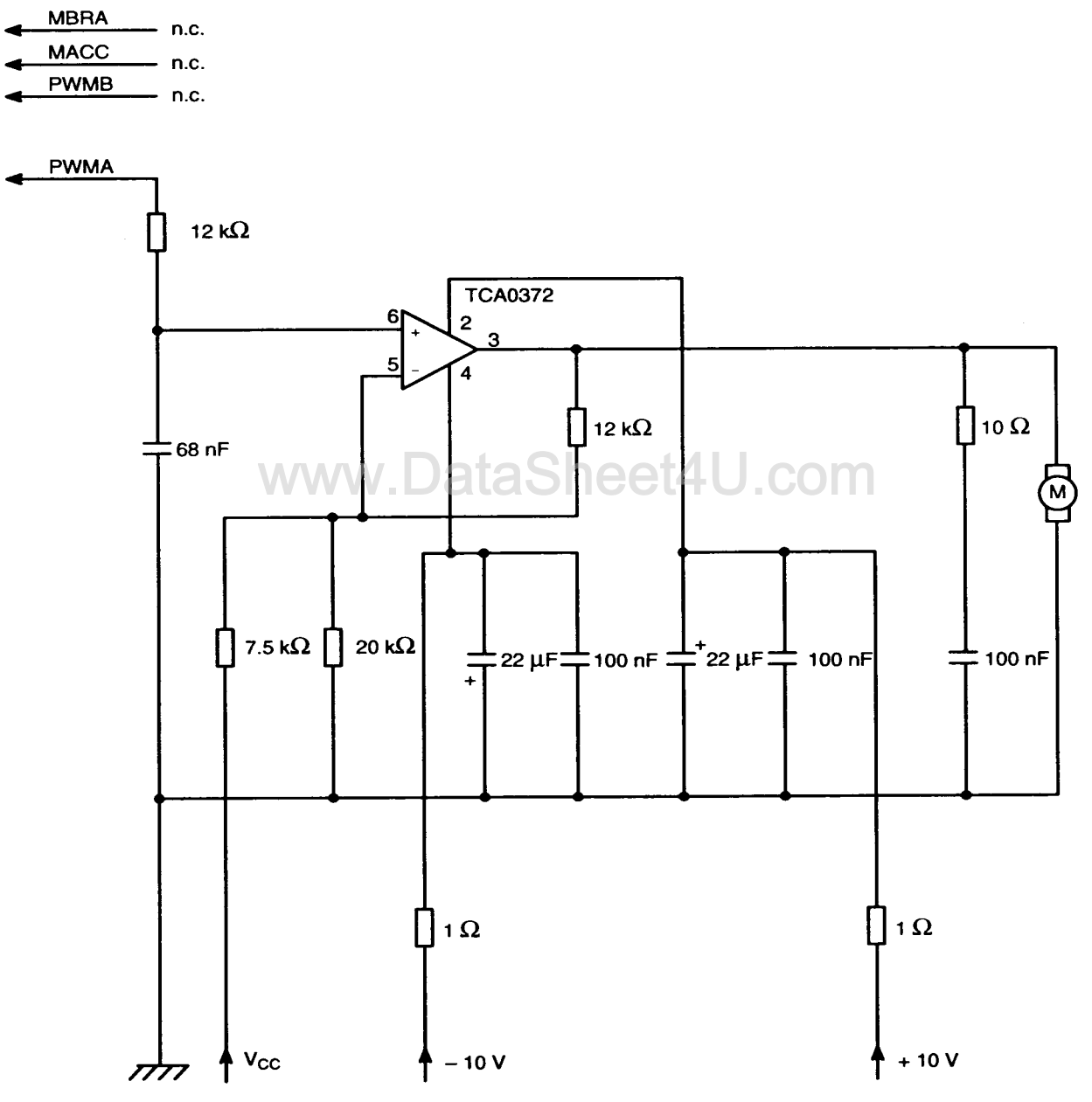


Fig.11 Motor interface; singled ended.

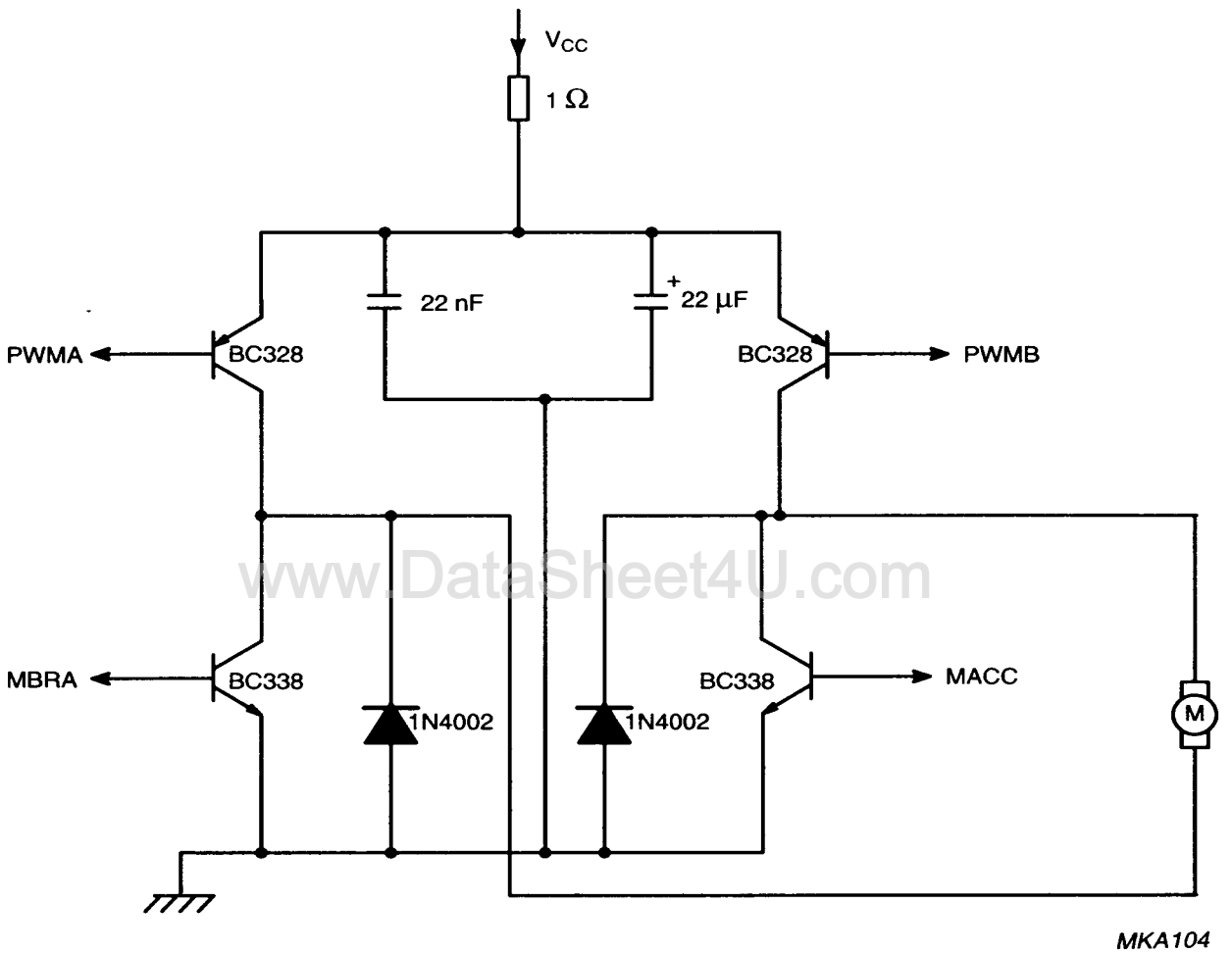
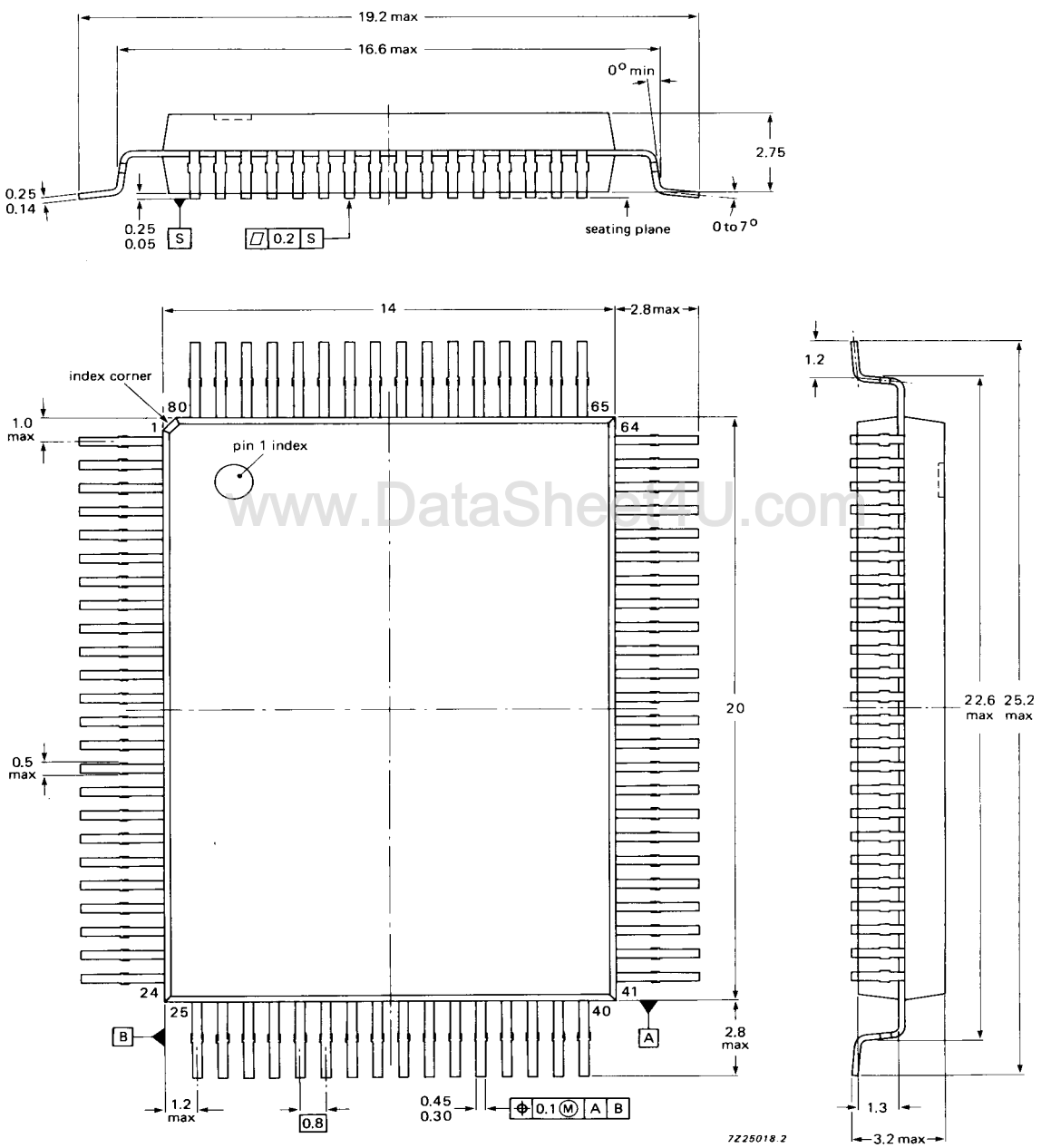


Fig.12 Motor interface; four wire.

PACKAGE OUTLINE



dimensions in mm

Fig.13 80-Lead quad flat-pack; plastic (SOT219)

SOLDERING

Plastic quad-flat pack

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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